# Thin Film Transistor LCD MODULE
# MODEL: AWK-240320T24N18
# Customer's No.:

| Acceptance |
|---|
| |

10-1 Floor, No. 192, Tahtung Road,
Sec. 3, Hsi-Chih Dist,
New Taipei City, Taiwan

| Approved and Checked by |
|---|
| |

| Approved by | Checked by | | Made by |
|---|---|---|---|
| 華叡 2023/03/08 NICK | 華叡 2023/03/08 JOE | | 華叡 2023/03/08 TOM |

# Revision Record

| Rev No. | Rev Date | Contents | Note |
|---|---|---|---|
| A | 2023/03/08 | New issue. | |
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# Table of Contents

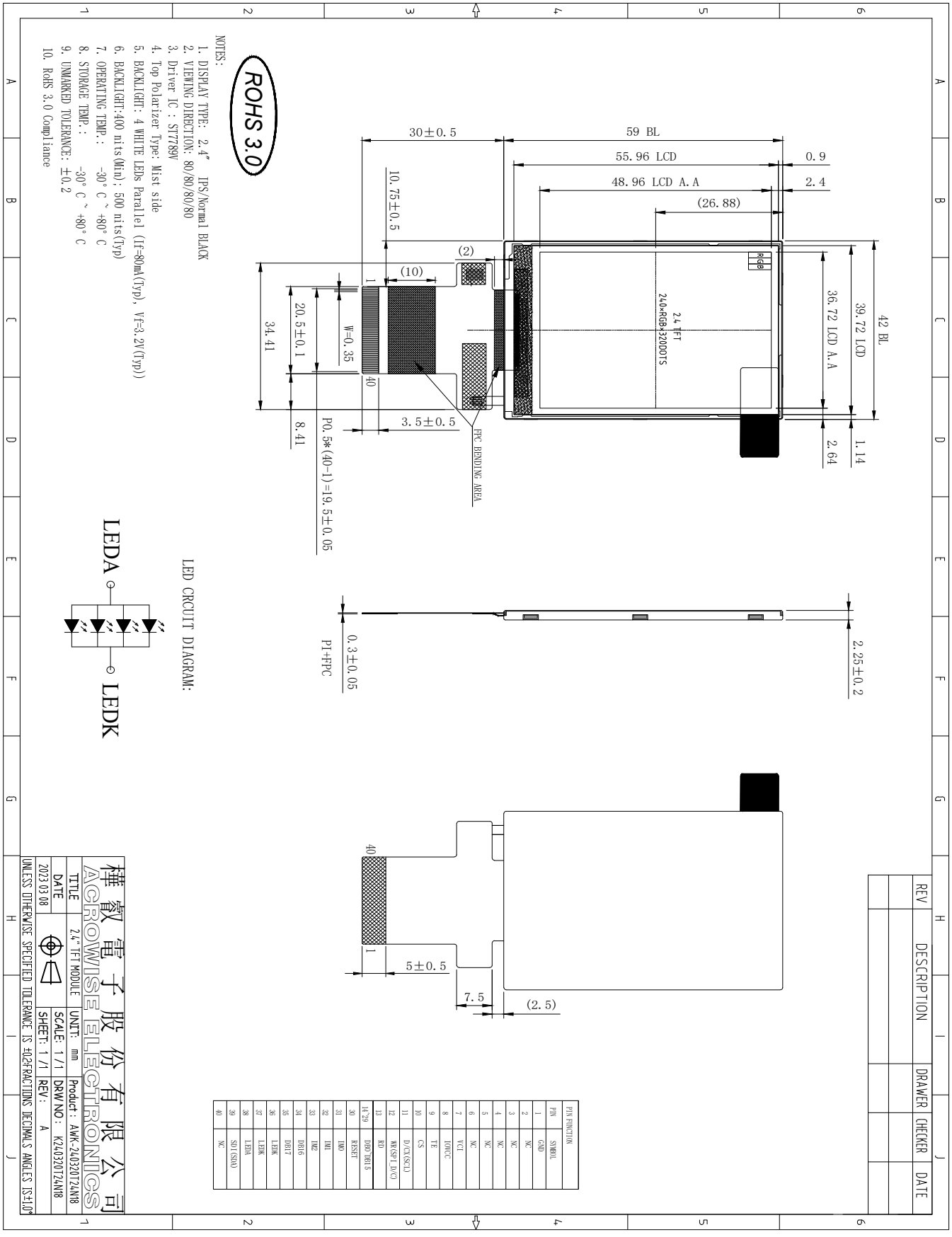
## 1. Scope

This specification defines general provisions as well as inspection standards for TFT module supplied by ACROWISE electronics. If the event of unforeseen problem or unspecified items may occur, naturally shall negotiate and agree to solution

## 2. General Information

| Item | Standard Values | Units |
|---|---|---|
| LCD type | 2.4”TFT | -- |
| Dot arrangement | 240 (RGB)×320 | dots |
| Color filter array | RGB vertical stripe | -- |
| Display mode | IPS/ Normally Black | - |
| Eyes Viewing Direction | 80/80/80/80 | |
| Driver IC | ST7789V | -- |
| Module size | 42(W)×59(H)×2.25(T) | mm |
| Active area | 36.72(W)×48.96(H) | mm |
| Dot pitch | 0.153(W)×0.153(H) | mm |
| Interface | 3SPI/4SPI&8/9/16/18bit MPU Parallel | -- |
| Operating temperature | -30 ~ +80 | °C |
| Storage temperature | -30 ~ +80 | °C |
| Back Light | 4 White LEDS | -- |

## 3. External Dimensions



## 4. Interface Description

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td></tr>
<tr><td>2~6</td><td>NC</td><td>No connection</td></tr>
<tr><td>7</td><td>VCI</td><td>High voltage power supply for analog circuit blocks (2.4~3.3V)</td></tr>
<tr><td>8</td><td>IOVCC</td><td>Low voltage power supply for interface logic circuits (1.65~3.3V)</td></tr>
<tr><td>9</td><td>TE</td><td>Tearing effect signal is used to synchronize MCU to frame memory writing.</td></tr>
<tr><td>10</td><td>CS</td><td>Chip selection pin<br>Low enable.<br>High disable.</td></tr>
<tr><td>11</td><td>D/CX(SCL)</td><td>This pin is used to be serial interface clock.<br>DCX=’1’: display data or parameter.<br>DCX=’0’: command data.</td></tr>
<tr><td>12</td><td>WR(SPI_D/C)</td><td>Write enable in MCU parallel interface.<br>Display data/command selection pin in 4-line serial interface.<br>Second Data lane in 2 data lane serial interface.<br>If not used, please fix this pin at IOVCC or GND.</td></tr>
<tr><td>13</td><td>RD</td><td>Read enable in 8080 MCU parallel interface.<br>If not used, please fix this pin at IOVCC or GND.</td></tr>
<tr><td>14~29</td><td>DB0~DB15</td><td>18-bit parallel bi-directional data bus for MCU system and RGB interface mode<br>If not used, please fix this pin at GND.</td></tr>
<tr><td>30</td><td>RESET</td><td>Reset pin. Initializes the IC, when this signal is low.<br>Must be reset after power is stable.</td></tr>
<tr><td>31</td><td>IM0</td><td rowspan="5"><table>
<tr><th>IM2</th><th>IM1</th><th>IM0</th><th>MPU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>80-8bit parallel I/F</td><td>DB[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>80-16bit parallel I/F</td><td>DB[15:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>80-9bit parallel I/F</td><td>DB[8:0]</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>80-18bit parallel I/F</td><td>DB[17:0],</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">0</td><td rowspan="2">1</td><td>3-line 9bit serial I/F</td><td>SDA: in/out</td></tr>
<tr><td>2 data lane serial I/F</td><td>SDA: in/out<br>WRX: in</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4-line 8bit serial I/F</td><td>SDA: in/out</td></tr>
</table></td></tr>
<tr><td>32</td><td>IM1</td></tr>
<tr><td>33</td><td>IM2</td></tr>
<tr><td>34</td><td>DB16</td><td>18-bit parallel bi-directional data bus for MCU system and RGB</td></tr>
</table>

| | | |
|---|---|---|
| 35 | DB17 | interface mode<br>If not used, please fix this pin at GND. |
| 36~37 | LEDK | LED backlight (Anode). |
| 38 | LEDA | LED backlight (Cathode). |
| 39 | SDI(SDA) | When IM[3]:Low, Serial in/out signal<br>When IM[3]:High, Serial input signal<br>The data is latched on the rising edge of the SCL signal.<br>If not used, please fix this pin at IOVCC or GND. |
| 40 | NC | No connection |

## 5. Absolute Maximum Ratings

| Item | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Logic Supply Voltage | IOVCC | -0.3 | 4.6 | V |
| Analog Supply Voltage | VCI | -0.3 | 4.6 | V |
| Input Voltage | Vin | -0.3 | IOVCC +0.5 | V |
| Operating Temperature | TOP | -30 | 80 | °C |
| Storage Temperature | TST | -30 | 80 | °C |
| Storage Humidity | HD | 20 | 90 | %RH |

## 6. DC Characteristics

| Item | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Logic Supply Voltage | IOVCC | 1.65 | 1.8 | 3.3 | V | - |
| Analog Supply Voltage | VCI | 2.4 | 2.75 | 3.3 | V | - |
| Logic Supply Current | IVCI | - | TBD | TBD | mA | - |
| Input High Voltage | $V_{IH}$ | 0.7 IOVCC | - | IOVCC | V | - |
| Input Low Voltage | $V_{IL}$ | GND | - | 0.3 IOVCC | V | - |
| Output High Voltage | $V_{OH}$ | 0.8 IOVCC | - | IOVCC | V | - |
| Output Low Voltage | $V_{OL}$ | -0.3 | - | 0.2 IOVCC | V | - |
| I/O Leak Current | ILI | -1 | - | 1 | uA | - |

# 7. Timing Characteristics

## 7.1 Power ON/OFF Sequence

VDDI and VDD can be applied in any order.

VDD and VDDI can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

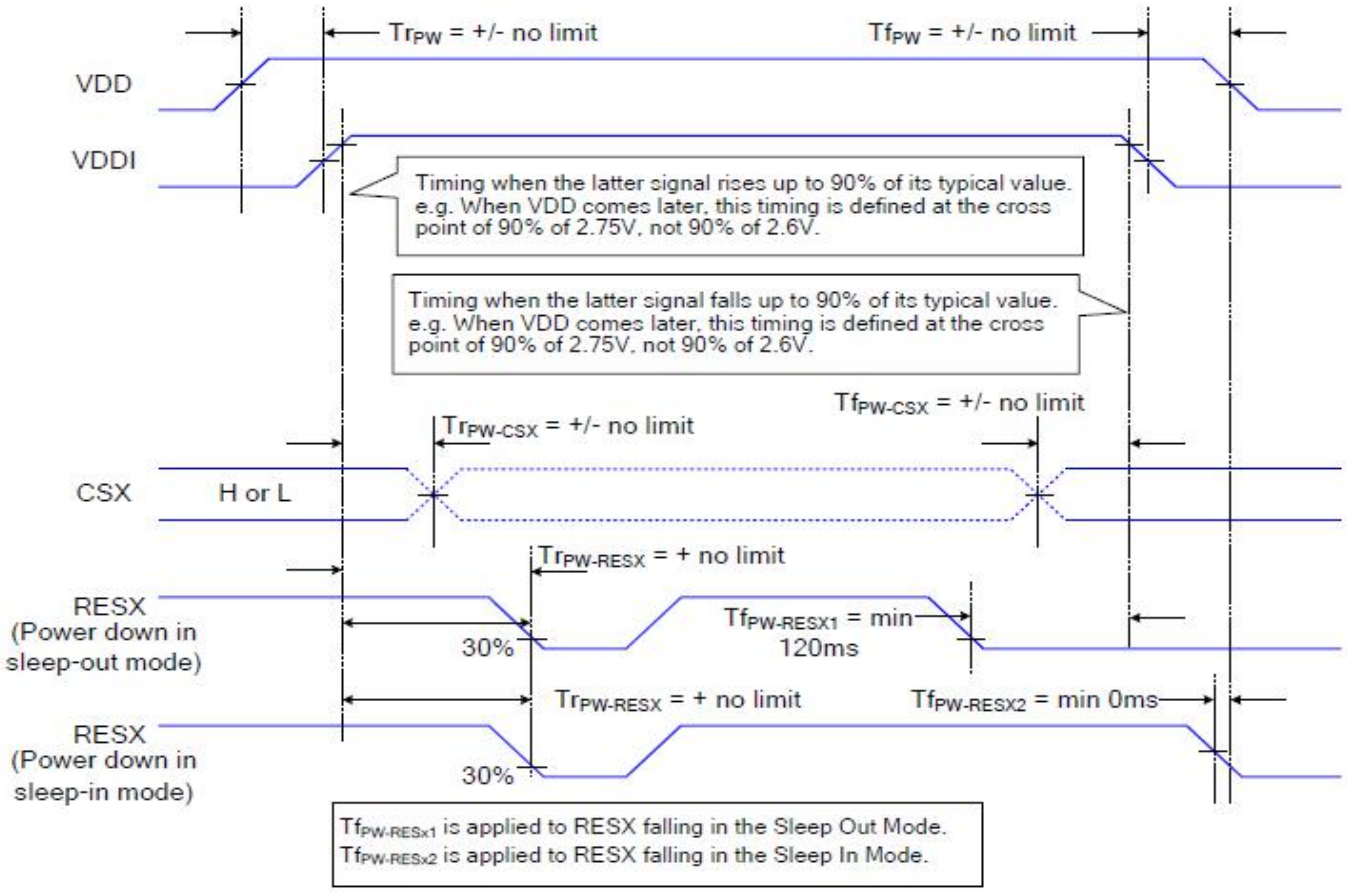
*Note 1: There will be no damage to the display module if the power sequences are not met.*

*Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*

*Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*

*Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*

The power on/off sequence is illustrated below



## 7.2 8080-System Interface Timing Characteristics(8/9/16/18bit)

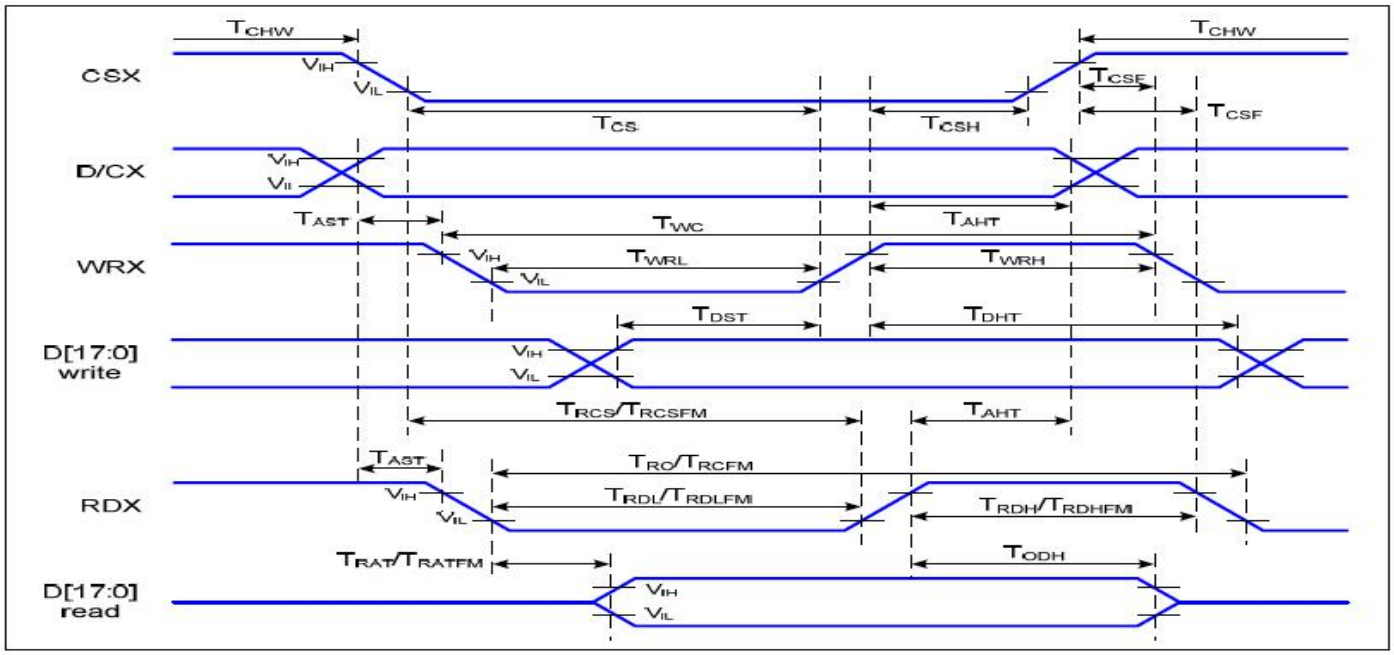



**Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)**

*VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃*

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| D/CX | $T_{AST}$ | Address setup time | 0 | | ns | - |
| | $T_{AHT}$ | Address hold time (Write/Read) | 10 | | ns | |
| CSX | $T_{CHW}$ | Chip select "H" pulse width | 0 | | ns | - |
| | $T_{CS}$ | Chip select setup time (Write) | 15 | | ns | |
| | $T_{RCS}$ | Chip select setup time (Read ID) | 45 | | ns | |
| | $T_{RCSFM}$ | Chip select setup time (Read FM) | 355 | | ns | |
| | $T_{CSF}$ | Chip select wait time (Write/Read) | 10 | | ns | |
| | $T_{CSH}$ | Chip select hold time | 10 | | ns | |
| WRX | $T_{WC}$ | Write cycle | 66 | | ns | |
| | $T_{WRH}$ | Control pulse "H" duration | 15 | | ns | |
| | $T_{WRL}$ | Control pulse "L" duration | 15 | | ns | |
| RDX (ID) | $T_{RC}$ | Read cycle (ID) | 160 | | ns | When read ID data |
| | $T_{RDH}$ | Control pulse "H" duration (ID) | 90 | | ns | |
| | $T_{RDL}$ | Control pulse "L" duration (ID) | 45 | | ns | |
| RDX (FM) | $T_{RCFM}$ | Read cycle (FM) | 450 | | ns | When read from frame memory |
| | $T_{RDHFM}$ | Control pulse "H" duration (FM) | 90 | | ns | |
| | $T_{RDLFM}$ | Control pulse "L" duration (FM) | 355 | | ns | |
| D[17:0] | $T_{DST}$ | Data setup time | 10 | | ns | For CL=30pF |

| | | | | | |
|---|---|---|---|---|---|
| | $T_{DHT}$ | Data hold time | 10 | | ns |
| | $T_{RAT}$ | Read access time (ID) | | 40 | ns |
| | $T_{RATFM}$ | Read access time (FM) | | 340 | ns |
| | $T_{ODH}$ | Output disable time | 20 | 80 | ns |

**Table 4 8080 Parallel Interface Characteristics**

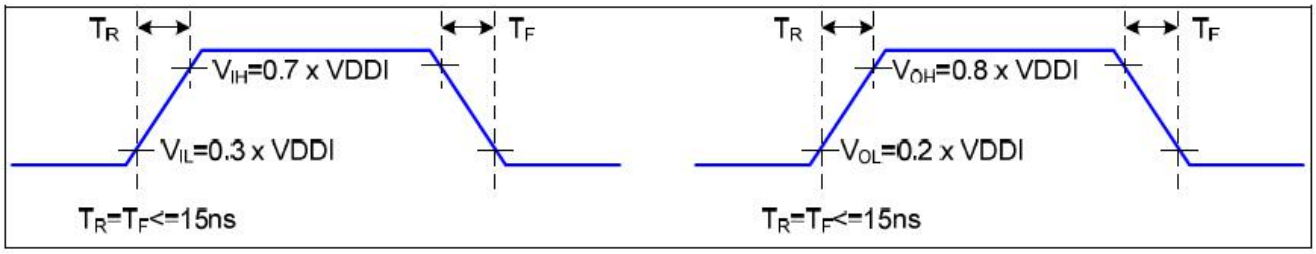



**Figure 2 Rising and Falling Timing for I/O Signal**

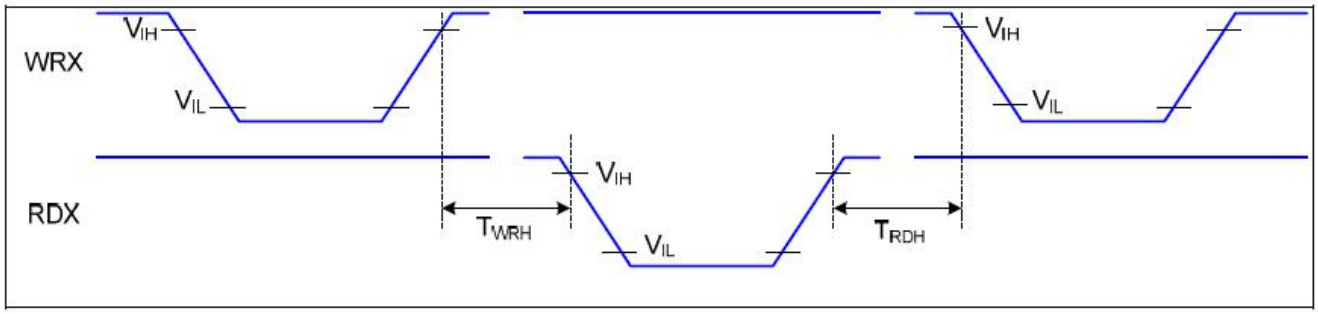
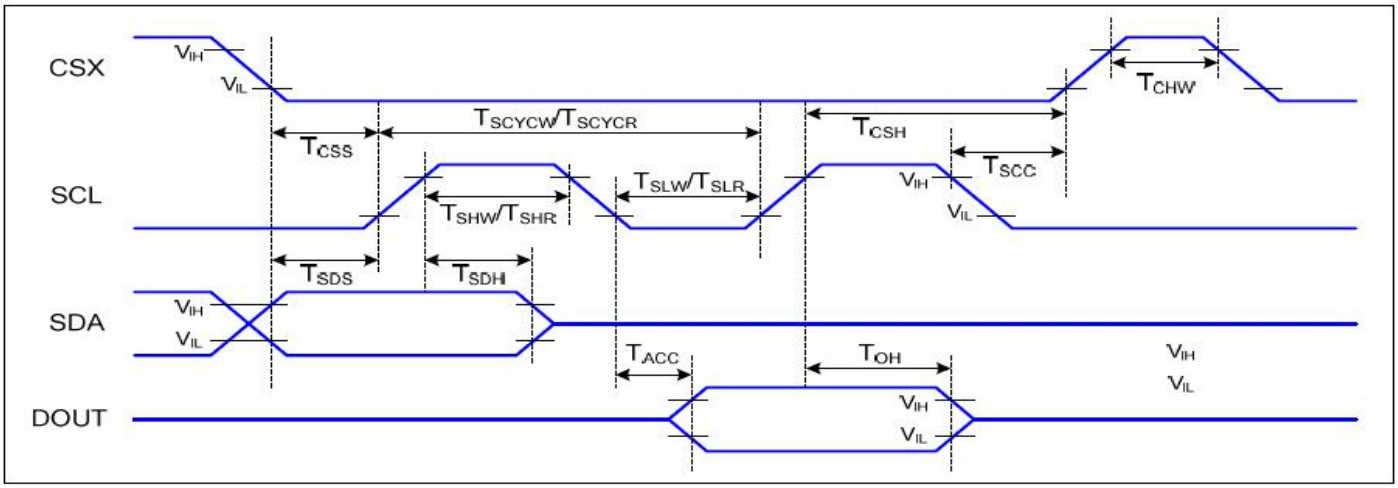



**Figure 3 Write-to-Read and Read-to-Write Timing**

*Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

## 7.3 Serial Interface Characteristics (3-line serial):



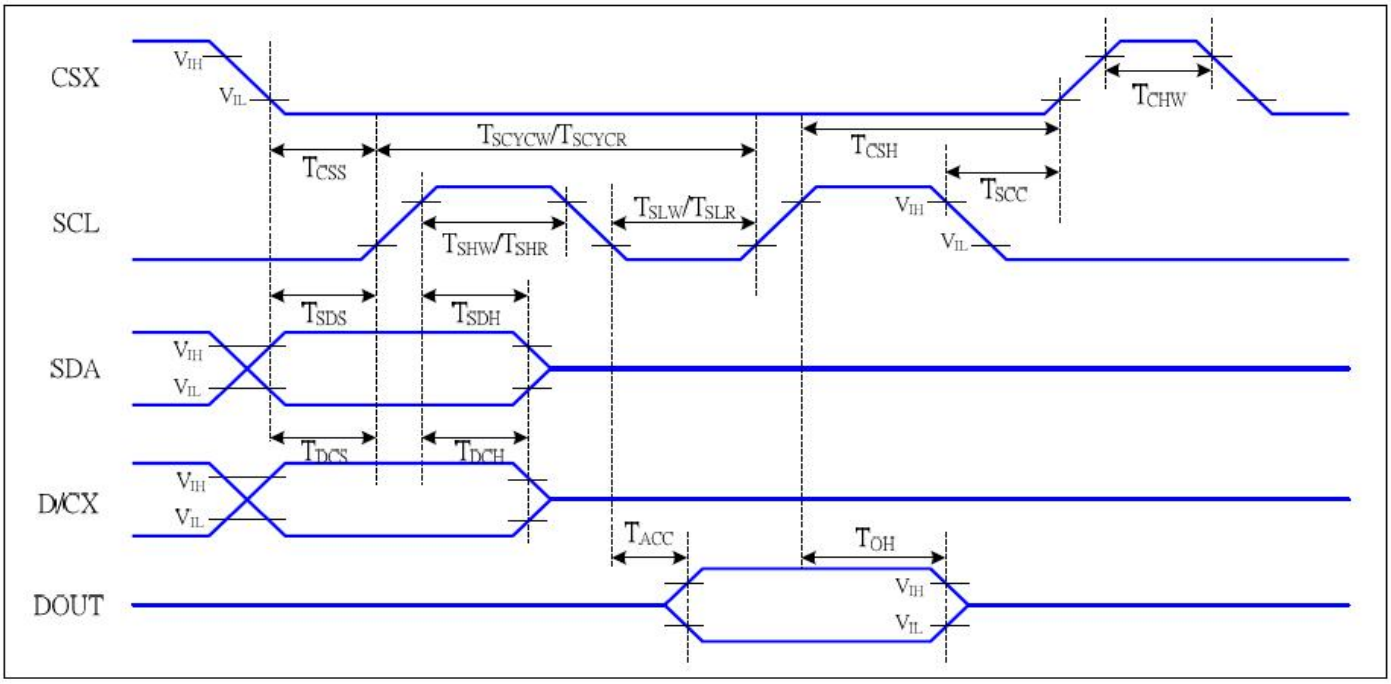

**3-line serial Interface Timing Characteristics**

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

| Signal | Symbol | Parameter | Min | Max | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | |
| | $T_{SHW}$ | SCL "H" pulse width (Write) | 15 | | ns | |
| | $T_{SLW}$ | SCL "L" pulse width (Write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | |
| | $T_{SHR}$ | SCL "H" pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (Read) | 60 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| DOUT | $T_{ACC}$ | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

**3-line serial Interface Characteristics**

## 7.4 Serial Interface Characteristics (4-line serial):




**4-line serial Interface Timing Characteristics**

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

| Signal | Symbol | Parameter | MIN | MAX | Unit | Description |
|---|---|---|---|---|---|---|
| CSX | $T_{CSS}$ | Chip select setup time (write) | 15 | | ns | |
| | $T_{CSH}$ | Chip select hold time (write) | 15 | | ns | |
| | $T_{CSS}$ | Chip select setup time (read) | 60 | | ns | |
| | $T_{SCC}$ | Chip select hold time (read) | 65 | | ns | |
| | $T_{CHW}$ | Chip select "H" pulse width | 40 | | ns | |
| SCL | $T_{SCYCW}$ | Serial clock cycle (Write) | 66 | | ns | -write command & data ram |
| | $T_{SHW}$ | SCL "H" pulse width (Write) | 15 | | ns | |
| | $T_{SLW}$ | SCL "L" pulse width (Write) | 15 | | ns | |
| | $T_{SCYCR}$ | Serial clock cycle (Read) | 150 | | ns | -read command & data ram |
| | $T_{SHR}$ | SCL "H" pulse width (Read) | 60 | | ns | |
| | $T_{SLR}$ | SCL "L" pulse width (Read) | 60 | | ns | |
| D/CX | $T_{DCS}$ | D/CX setup time | 10 | | ns | |
| | $T_{DCH}$ | D/CX hold time | 10 | | ns | |
| SDA (DIN) | $T_{SDS}$ | Data setup time | 10 | | ns | |
| | $T_{SDH}$ | Data hold time | 10 | | ns | |
| DOUT | $T_{ACC}$ | Access time | 10 | 50 | ns | For maximum CL=30pF |
| | $T_{OH}$ | Output disable time | 15 | 50 | ns | For minimum CL=8pF |

**4-line serial Interface Characteristics**

## 7.5Reset Timing

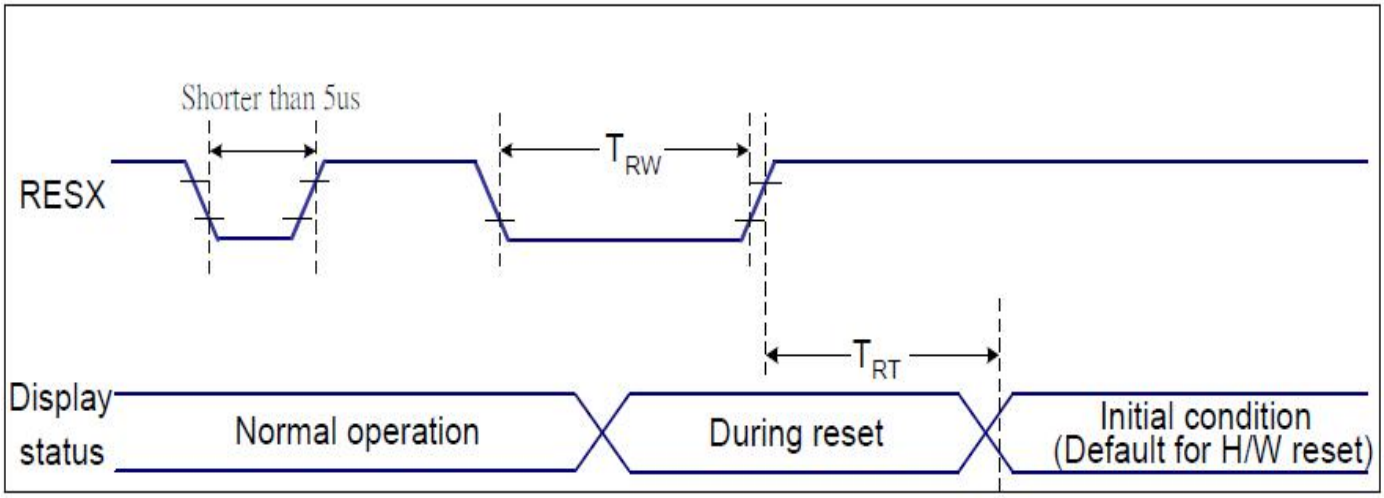



**Figure 7 Reset Timing**

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

| Related Pins | Symbol | Parameter | MIN | MAX | Unit |
|---|---|---|---|---|---|
| RESX | TRW | Reset pulse duration | 10 | - | us |
| | TRT | Reset cancel | - | 5 (Note 1, 5) | ms |
| | | | | 120 (Note 1, 6, 7) | ms |

**Table 9 Reset Timing**

*Notes:*

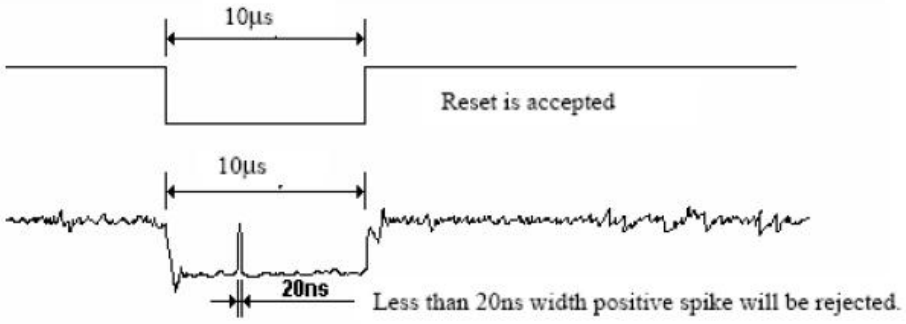
*1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.*

*2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:*

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 9us | Reset |
| Between 5us and 9us | Reset starts |

*3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.*

*4. Spike Rejection also applies during a valid reset pulse as shown below:*

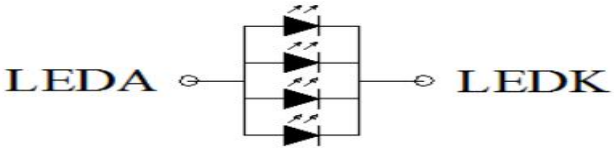



*5. When Reset applied during Sleep In Mode.*

*6. When Reset applied during Sleep Out Mode.*

*7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.*

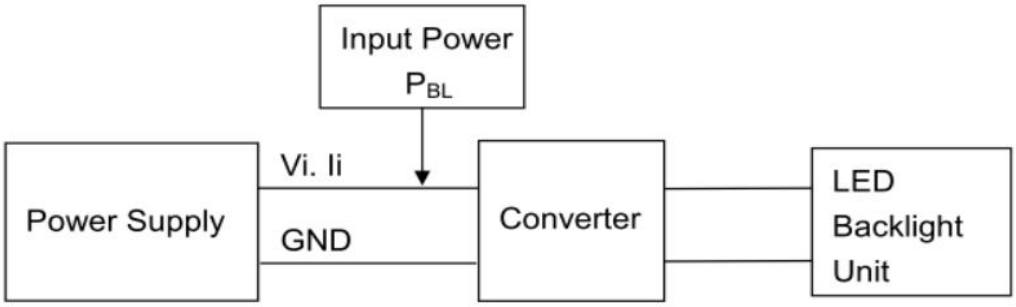
## 8. Backlight Characteristic




| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| Supply Voltage | Vf | 2.7 | 3.2 | 3.5 | V | Note 1 |
| Supply Current | If | - | 80 | - | mA | Note 2 |
| Life Time | - | - | 30000 | - | Hr | Note 3,4 |
| Backlight Color | White | | | | | |

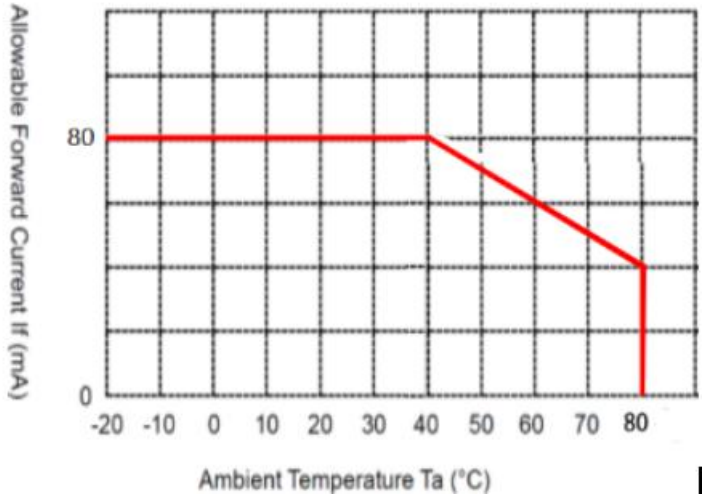
**Note 1:** The LED Supply Voltage is defined by the number of LED at Ta=25℃ and If = 80mA.

**Note 2:** LED current is measured by utilizing a high frequency current meter as shown below:




**Note 3:** The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and If = 80mA. The LED lifetime could be decreased if operating If is larger than 80mA.

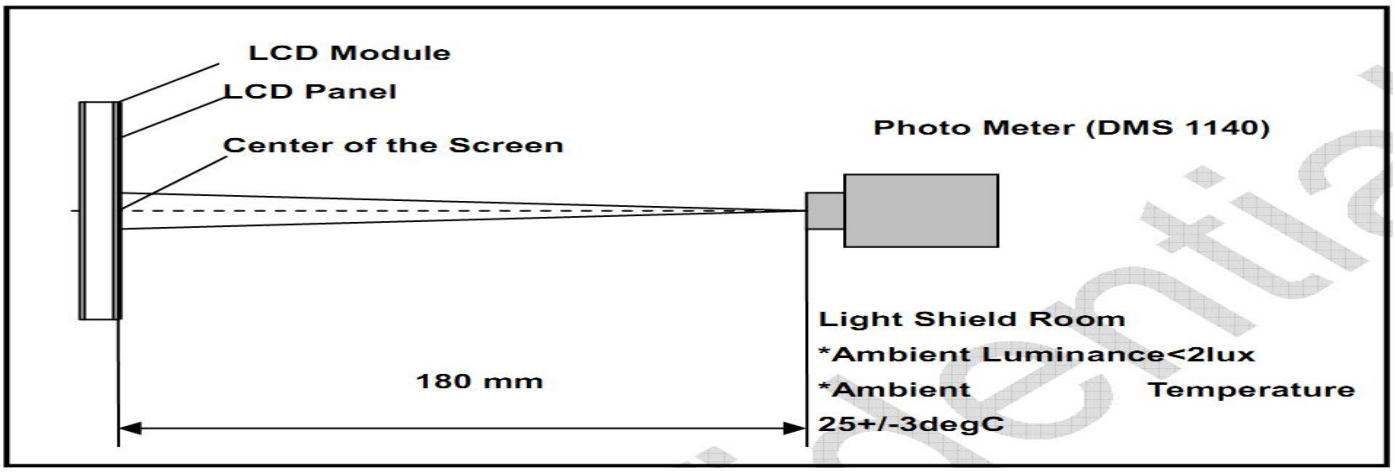
**Note 4:** LED light bar circuit:



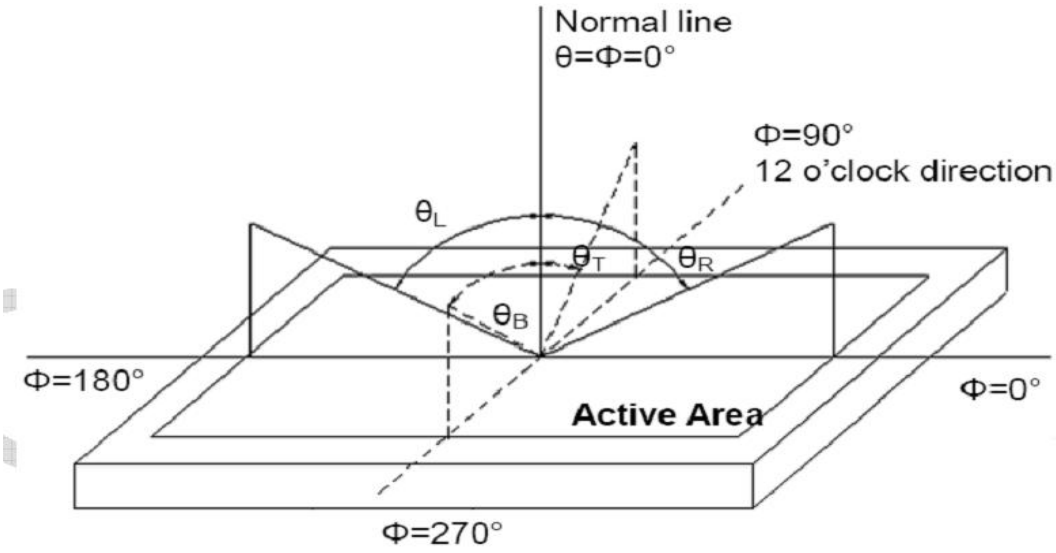
## 9. Optical Characteristics

| Item | Conditions | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Viewing Angle (CR>10) | Horizontal | θL | - | 80 | - | degree | (1),(2),(6) |
| | | θR | - | 80 | - | | |
| | Vertical | θT | - | 80 | - | | |
| | | θB | - | 80 | - | | |
| Luminous Intensity for LCM | - | | 400 | 500 | - | cd/m2 | |
| Uniformity for LCM | - | | 75 | 80 | - | % | |
| Contrast Ratio | Center | | 600 | 800 | - | - | (1),(3),(6) |
| Response Time | Rising | | - | 16 | 21 | ms | (1),(4),(6) |
| | Falling | | - | 19 | 24 | | |
| CF Color Chromaticity (CIE1931) | White x | | TBD | TBD | TBD | | |
| | White y | | TBD | TBD | TBD | | |
| | Red x | | TBD | TBD | TBD | | |
| | Red y | | TBD | TBD | TBD | | |
| | Green x | | TBD | TBD | TBD | | |
| | Green y | | TBD | TBD | TBD | | |
| | Blue x | | TBD | TBD | TBD | - | |
| | Blue y | | TBD | TBD | TBD | - | |

**Note (1) Measurement Setup:** The LCD module should be stabilized at given temp. 25°C for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



**Note (2) Definition of Viewing Angle**



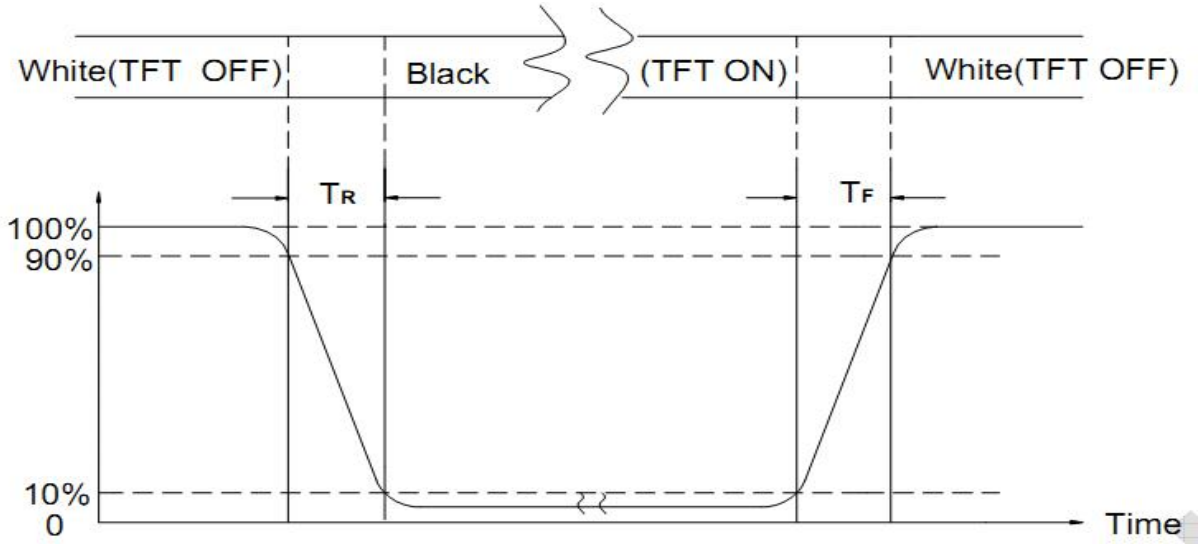

**Note (3) Definition of Contrast Ratio (CR)**

The contrast ratio can be calculated by the following expression

Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

**Note (4) Definition of response time**




**Note (5)** Definition of Transmittance (Module is without signal input)

Transmittance = Center Luminance of LCD / Center Luminance of Back Light x 100%

**Note (6)** Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD

## 10. Reliability Test Conditions and Methods

| No. | Test Items | Test Condition | Inspection After Test |
|---|---|---|---|
| ① | High Temperature Storage | 80°C±2°C×96Hours | Inspection after 2~4hours storage at room temperature, the samples should be free from defects:<br>1, Air bubble in the LCD.<br>2, Seal leak.<br>3, Non-display.<br>4, Missing segments.<br>5, Glass crack.<br>6, Current IDD is twice higher than initial value.<br>7, The surface shall be free from damage.<br>8, The electric characteristic requirements shall be satisfied. |
| ② | Low Temperature Storage | -30°C±2°C×96Hours | |
| ③ | High Temperature Operating | 80°C±2°C×96Hours | |
| ④ | Low Temperature Operating | -30°C±2°C×96Hours | |
| ⑤ | Temperature Cycle(Storage) | -30°C (30min) ⇔ 25°C (5min) ⇔ 80°C (30min)<br>1cycle<br>Total 10cycle | |
| ⑥ | Damp Proof Test (Storage) | 50°C±5°C×90%RH×96Hours | |
| ⑦ | Vibration Test | Frequency:10Hz~55Hz~10Hz<br>Amplitude:1.5mm<br>X,Y,Z direction for total 3hours<br>(packing condition test will be tested by a carton) | |
| ⑧ | Drooping Test | Drop to the ground from 1M height one time<br>every side of carton.<br>(packing condition test will be tested by a carton) | |
| ⑨ | ESD Test | Voltage:±8KV,R:330Ω,C:150PF,Air Mode,10times | |

REMARK:
1, The Test samples should be applied to only one test item.
2, Sample side for each test item is 5~10pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5, EL evaluation should be accepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6, Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

# 11. Inspection Standard

## 11.1 Scope

Specifications contain

11.1.1 Display Quality Evaluation

11.1.2 Mechanics Specification

## 11.2 Sampling Plan

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E.

11.2.1 Lot size: Quantity per shipment as one lot (different model as different lot ).

11.2.2 Sampling type: Normal inspection, single sampling.

11.2.3 Sampling level: Level II.

11.2.4 AQL: Acceptable Quality Level

ISO-2859-I(SAME AS MIL-STD-105E), LECEL II SINGLE PLAN.

| CLASS | AQL(%) |
|---|---|
| CRITICAL | 0.4 % |
| MAJOR | 0.65 % |
| MINOR | 1.5 % |
| TOTAL | 1.5 % |

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

## 11.3 Panel Inspection Condition

11.3.1 Environment:

Room Temperature: 25±5°C. Humidity: 65±5% RH. Illumination: 300 ~ 700 Lux.

11.3.2 Inspection Distance: 35±5 cm

11.3.3 Inspection Angle:

The vision of inspector should be perpendicular to the surface of the Module.

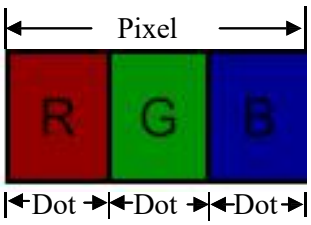
11.3.4 Inspection time:

Perceptibility Test Time: 20 seconds max.

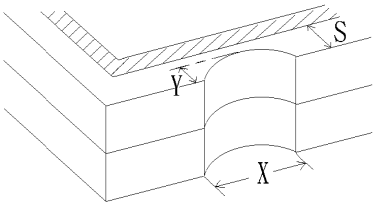
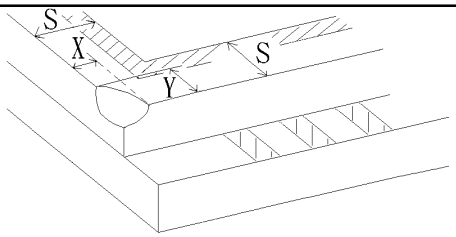
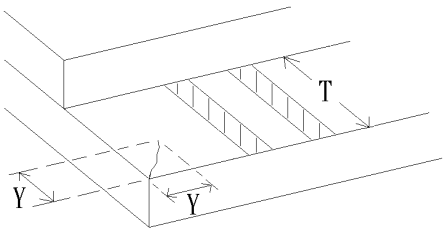
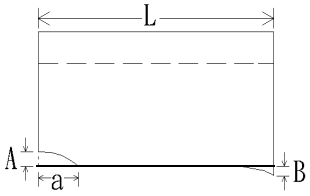
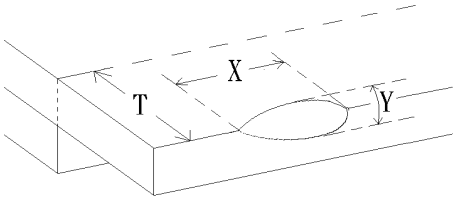
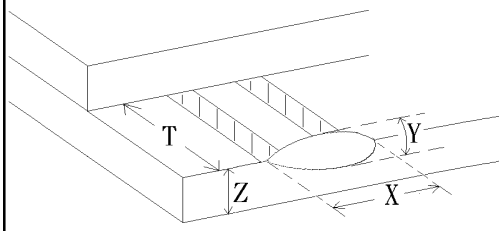
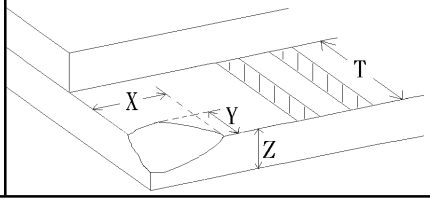
## 11.4 Inspection Plan

| Class | Item | Judgment | Class |
|---|---|---|---|
| Packing & Indicate | 1. Outside and inside package. | "MODEL NO.", "LOT NO." and "QUANTITY" should indicate on the package. | Minor |
| | 2. Model mixed and quantity. | Other model mixed<br>Quantity short or over | CRITICAL |
| | 3. Product indication. | "MODEL NO." should indicate on the product. | Major |
| Assembly | 4. Dimension,<br>LCD glass scratch and scribe defect. | According to specification or drawing. | Major |
| Appearance | 5. Viewing area. | Polarizer edge or LCD's sealing line is visable in the viewing area…….Rejected. | Minor |
| | 6. Blemish, black spot, white spot in the LCD and LCD glass cracks. | According to standard of visual inspection.(inside viewing area) | Minor |
| | 7. Blemish, black spot, white spot and scratch on the polarizer. | According to standard of visual inspection.(inside viewing area) | Minor |
| | 8. Bubble in polarizer. | According to standard of visual inspection.(inside viewing area) | Minor |
| | 9. LCD's rainbow color. | Strong deviation color (or newton ring) of LCD…….....Rejected.<br>Or according to limited sample.(if needed, and inside viewing area) | Minor |
| Electrical | 10. Electrical and optical characteristics.(contrast Vop chromaticity….etc) | According to specification or drawing.(inside viewing area) | CRITICAL |
| | 11. Missing line. | Missing dot line character | CRITICAL |
| | 12.Short circuit.<br>Wrong pattern display. | No display, wrong pattern display, current consumption.<br>Out of specification | CRITICAL |
| | 13. Dot defect.(for color and TFT) | According to standard of visual Inspection. | Minor |

## 11.5 Standard Of Visual Inspection

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGMENT</th></tr>
<tr><td>11.5.1</td><td>Minor</td><td>Black and white spot.<br>Foreign materiel.<br>Dust.<br>Blemish.<br>Scratch.</td><td>(A) Round type: Unit: mm
<table>
<tr><th>Diameter (mm.)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.2</td><td>Disregard</td></tr>
<tr><td>0.2 < Φ≦0.35</td><td>2(Distance>5mm)</td></tr>
<tr><td>0.35 < Φ</td><td>0</td></tr>
</table>
Note: Φ = (length+width)/2<br>(B) Linear type: Unit: mm
<table>
<tr><th>Length</th><th>Width (mm.)</th><th>Acceptable Q'ty</th></tr>
<tr><td>--</td><td>W≦0.03</td><td>Disregard</td></tr>
<tr><td>L≦5.0</td><td>0.03< W≦0.05</td><td>2(Distance>5mm)</td></tr>
<tr><td>--</td><td>0.05 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>11.5.2</td><td>Minor</td><td>Dent on polarizer.</td><td>Unit: mm.
<table>
<tr><th>Diameter</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.2</td><td>Disregard</td></tr>
<tr><td>0.2 < Φ≦0.5</td><td>2(Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>11.5.3</td><td>Minor</td><td>Bubble in polarizer.</td><td>Unit: mm.
<table>
<tr><th>Diameter</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.2</td><td>Disregard</td></tr>
<tr><td>0.2< Φ≦0.5</td><td>2(Distance>5mm)</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>11.5.4</td><td>Minor</td><td>Dot defect</td><td>
<table>
<tr><th>Items</th><th>Acceptable Q'ty</th></tr>
<tr><td>Bright dot</td><td>N ≦1</td></tr>
<tr><td>Dark dot</td><td>N ≦1</td></tr>
<tr><td>Total dot</td><td>N ≦2</td></tr>
</table>
Pixel define : 

Note1: The definition of dot: The size of a defective dot over 1/2 of whole dot is regarded as one defective dot.<br>Note 2: Bright dot: Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.<br>Note 3: The bright dot defect must be visible through 2% ND filter<br>Note 4: Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue pattern.</td></tr>
</table>

| No. | Class | Item | Judgment |
|---|---|---|---|
| 11.5.5 | Minor | LCD glass chipping. |   Y>S Reject |
| 11.5.6 | Minor | LCD glass chipping. |   X or Y>S Reject |
| 11.5.7 | Major | LCD glass crack. |   Y>(1/2) T Reject |
| 11.5.8 | Major | LCD glass scribe defect. |   1. a>L/3, A>1.5mm Reject<br>2. B : According to dimension |
| 11.5.9 | Minor | LCD glass chipping.<br>(on the terminal area) |   Φ = (x+y)/2>2.5mm Reject |
| 11.5.10 | Minor | LCD glass chipping.<br>(on the terminal surface) |   Y>(1/3)T Reject |
| 11.5.11 | Minor | LCD glass chipping. |   Y>T Reject |

# 12. Handling Precautions

## 12.1 Mounting Method

The LCD panel of ACROWISE TFT module consists of two thin glass plates with polarizes which easily be damaged. And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board.

Extreme care should be needed when handling the LCD modules.

## 12.2 Caution of LCD Handling And Cleaning

When cleaning the display surface, Use soft cloth with solvent

[Recommended below] and wipe lightly

- Isopropyl alcohol
- Ethyl alcohol

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Aromatics

Do not wipe ITO pad area with the dry or hard materials that will damage the ITO patterns

Do not use the following solvent on the pad or prevent it from being contaminated:

- Soldering flux
- Chlorine (Cl) , Sulfur (S)

If goods were sent without being silicon coated on the pad, ITO patterns could be damaged due to the corrosion as time goes on.

If ITO corrosion happen by miss-handling or using some materials such as Chlorine (CI), Sulfur (S) from customer, Responsibility is on customer.

## 12.3 Caution Against Static Charge

The LCD module use C-MOS LSI drivers, so we recommended that you:

Connect any unused input terminal to power or ground, do not input any signals before power is turned on, and ground your body, work/assembly areas, and assembly equipment to protect against static electricity.

## 12.4 Packing

- Module employs LCD elements and must be treated as such.
- Avoid intense shock and falls from a height.
- To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity

## 12.5 Caution for operation

- It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage then the limit cause the shorter LCD life.
- An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current drive should be avoided.
- Response time will be extremely delayed at lower temperature then the operating temperature range and on the other hand at higher temperature LCD's how dark color in them. However those phenomena do not mean malfunction or out of order with LCD's, which will come back in the specified operation temperature.
- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.
- Slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

  Usage under the maximum operating temperature, 50%Rh or less is required.

## 12.6 Storing

In the case of storing for a long period of time for instance, for years for the purpose or replacement use, the following ways are recommended.

- Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with no desiccant.
- Placing in a dark place where neither exposure to direct sunlight nor light's keeping the storage temperature range.
- Storing with no touch on polarizer surface by the anything else.

  [It is recommended to store them as they have been contained in the inner container at the time of delivery from us

## 12.7 Safety

- It is recommendable to crash damaged or unnecessary LCD's into pieces and wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.
- When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water

## 13. Precaution for Use

### 13.1

A limit sample should be provided by the both parties on an occasion when the both parties agreed its necessity. Judgment by a limit sample shall take effect after the limit sample has been established and confirmed by the both parties.

### 13.2

On the following occasions, the handing of problem should be decided through discussion and agreement between responsible of the both parties.

- When a question is arisen in this specification
- When a new problem is arisen which is not specified in this specifications
- When an inspection specifications change or operating condition change in customer is reported to ACROWISE TFT , and some problem is arisen in this specification due to the change
- When a new problem is arisen at the customer's operating set for sample evaluation in the customer site.